REMARKS

With respect to the objection to claim 9, claim 9 has been amended.

With respect to the objection to claim 15, claim 15 has been amended.

With respect to the objection to claim 17, claim 17 has been amended.

With respect to the objection to claim 20, the item 55, in Figure 14, meets the claimed limitations. Reconsideration is requested.

Claim 21 was rejected over the previously cited reference. The omission of the translation is regretted.

However, it is noted that the material 4 is actually the phase change material. It would not constitute a via under any reasonably accepted definition adopted by one skilled in the art. As evidence thereof, a copy of the definition of a via from the Online Semiconductor Glossary is attached.

Reconsideration of the rejection of claim 21 is respectfully requested.

Likewise, reconsideration of the rejection of claim 27 is requested in view of the translation. The layer 16 is not between the threshold switch and the phase change memory. The layer 16 is an insulating layer which is part of the memory element 9. There is no barrier layer between the memory element 9 and the decoupling element 10.

With respect to claim 1, the claim has been amended to preclude the interpretation suggested of periphery. It is further noted that periphery is a term of art and it refers to an area outside the memory area. One skilled in the art would have this understanding. Nonetheless, the claim has been amended to preclude the interpretation suggested in the office action.

Therefore, reconsideration is respectfully requested.

In view of these remarks, the application is now in condition for allowance.

Respectfully submitted,

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Term (Index)	Definition
via	hole etched in the interlayer dielectric which is then filled with metal, usually tungsten, to provide vertical connection between stacked up interconnect metal lines.

Term (Index)	Definition
via veil	residue resulting from the resist stripping process following via etch in multilevel interconnect scheme

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